

Press Release

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BESANG, NATIONAL NANOFAB CENTER, AND STANFORD UNIVERSITY NANOFAB DEVELOP BREAKTHROUGH 3D IC TECHNOLOGY



Seoul, Korea – In collaboration with the National Nanofab Center (NNFC) in Daejeon, Korea and Stanford Nanofab (SNF) in Palo Alto, CA, BeSang Inc., a semiconductor company based in Beaverton, OR, has successfully developed a breakthrough three-dimensional (3D) integrated circuit (IC) technology, enabling low-cost memories and high-performance logic products with large embedded memory blocks.

This 3D IC has been processed on 8 inch wafers with industry standard 0.18 μm CMOS technologies both at NNFC and SNF. The chip contains 128 million vertically oriented devices as a test vehicle. It is uniquely processed at low temperatures, below 400 degree Celsius. A submicron thick single crystalline silicon layer is initially formed above the silicon substrate with two metal interconnect layers, followed by vertical devices and additional metal layer.

“Collaboration with BeSang on 3D IC development demonstrates the expert technical capability of NNFC and the commercialization of emerging semiconductor technologies. We expect that BeSang’s breakthrough 3D IC technology will provide ultimate low-cost and high-performance solutions for the semiconductor industry,” said Dr. Hee Chul Lee, president of NNFC and professor of Korea Advanced Institute of Science & Technology. “I am pleased that BeSang’s 3D IC development is the first success story of excellent collaboration and technology exchange between SNF and NNFC.”

Unlike conventional semiconductor technologies with planar devices on the surface of the semiconductor substrate and interconnects only above the planar devices, this emerging 3D IC technology forms full 3D interconnects below and above the vertical devices. This represents a significant breakthrough.

“One of unique features of BeSang’s 3D IC is the capability of unrestricted 3D interconnections using conventional via technologies that does not require wafer alignment nor through-silicon vias for 3D interconnects,” said Dr. Yoshio Nishi, head of SNF and professor at Stanford University. “Conventional CMOS technology is facing its scaling limits. Therefore, this emerging 3D IC technology will extend the lifespan of CMOS technology, because it is an excellent alternative way to accommodate more devices on a given wafer area.”

Chip level 3D IC has been explored for many years by the semiconductor industry. However, market introduction of chip level 3D IC has been delayed due to technical challenges, including high-temperature processing, defects in semiconductor layers, limited 3D interconnections, and a complex process. For the first time in the industry, BeSang provides solutions to these problems and has successfully generated high-performance and reliable devices on single crystalline silicon layers that are subsequently formed above another silicon substrate at low temperature. The low-temperature, high performing process is an important aspect of this new technology.

“BeSang’s 3D IC is a novel combination of short process steps, formation of array blocks in 3D, thin layer transfer using unique wafer bonding, followed by low temperature processing,” said Dr. Simon Sze, professor at National Chiao Tung University. “Hence, there is a high possibility for this breakthrough 3D IC to provide low-cost manufacturing solutions for the semiconductor industry. BeSang’s 3D IC is a very attractive technology and one wonders why other companies have not thought about it. However, I always believe in the dynamics of small companies as my colleague, Dawon Kahng, and I worked as a small team within a large organization when we co-invented the non-volatile memory in 1967 at Bell Labs.”

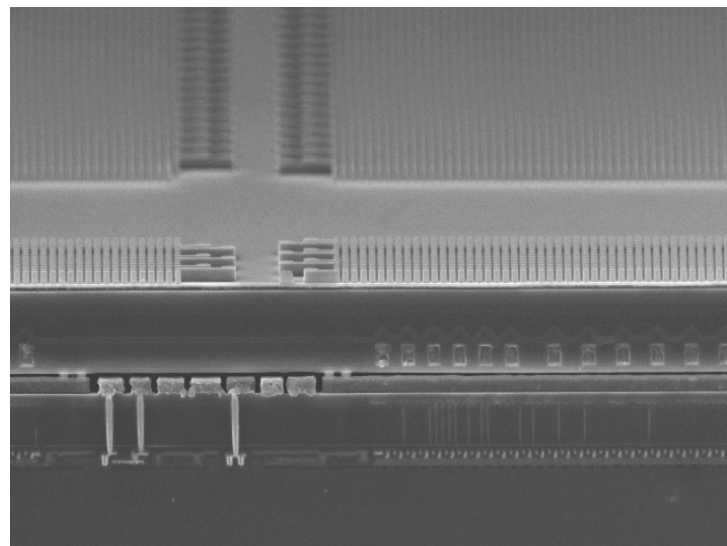
“We can imagine evolution of semiconductor technologies through 3D vertical stacking instead of conventional horizontal shrinking which is getting more expensive and facing ever more technical difficulties,” said Dr. Dieter Schroder, professor at Arizona State University and on the board of directors of BeSang.

This 3D IC concept has been successfully demonstrated by BeSang at SNF in early 2007 and has been further developed at the commercial level technologies at NNFC since July 2007.

“For rapid wafer processing, engineers at NNFC and students and staff members at SNF reserved the tools for BeSang. With such strong support from NNFC and SNF, BeSang has successfully reached this level of technology development in a very short time. I would like to say special thanks to all at NNFC and SNF,” said Sang-Yun Lee, CEO of BeSang.

BeSang’s 3D IC technology with vertical devices aims at an innovative, simpler, and more cost-effective way to enhance large functional blocks, such as memory arrays or photodiodes for image sensors, systems-on-a-chip, microprocessors, and memory control logic circuitry in advanced semiconductor chips.

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About BeSang. BeSang is a fabless semiconductor company developing its proprietary 3D memory technology. The Company will enter the semiconductor memory business for both the stand-alone and embedded memory markets. The main mission of the Company is to provide unique and sustainable technical solutions that can significantly reduce manufacturing costs of semiconductor chips including ultra high-density memories. BeSang has developed high-value intellectual property related to this technology, which will be useful for companies in the microprocessor, system-on-a-chip (SoC), and stand-alone memory markets. For more information, visit the BeSang Website at <http://www.BeSang.com>.

About NNFC. National NanoFab Center (NNFC) is an advanced nanotechnology laboratory located in Daejeon, Korea and started the service to the users in March 2005. NNFC's mission is to support R&D activities to verify basic ideas which are not supported by existing foundry companies and to offer a cooperating bridge between research communities with the following strengths: equipments necessary to carry out R&D in the field of nanotechnology, years of industry-experienced human resources, many collaborative programs with industry in CMOS, MEMS, and nanomaterials to commercialize their ideas, and a worldwide network of cooperation and technology. NNFC covers integration and fusion of Si-CMOS, MEMS, Biochip technologies, and nanomaterials, and supports wide range from the basic idea verification, to the prototype, and to the engineering sample, and provides wide process capability from piece to 8 inch wafer for various users.

About SNF. The Stanford Nanofabrication Facility (SNF) is a state-of-the-art, shared-equipment laboratory open to academic, industrial and governmental researchers. The 10,500 ft² cleanroom is located on the campus of Stanford University (Palo Alto, Calif.). Over 600 registered lab members research technologies ranging from MEMS, optics, biology and chemistry to traditional electronic device fabrication and process characterization. In this environment, personnel with expertise in process equipment assist in transforming ideas into working devices. Since opening in 1985, hundreds of projects have successfully passed through the SNF.